IN THE SPECIFICATION

Page 28, sixth full paragraph (lines 24-28), please amend as follows:

It is assumed that the memory cells MC0 to MC7 holding a data string including data for one byte first output from the data input/output terminal group 10 hold data "11", ~~"01", "00"~~ "00", "01", "10", "00", "01", ~~"01", "00"~~ "10" and "11" respectively. Therefore, the data latch circuit DL-L holds data C9h in hexadecimal notation in an area for one byte.

Page 43, Table 2, please amend as follows:

Table 2

Write Mode		Gate Voltage (Word Line Voltage)	Drain Voltage	Source Voltage
Writing at Level 4	write bit sense latch: "0" data latch: "0" in DL-L, "1" in ~~or~~ DL-R	VW4 (e.g., 17V)	V1 (e.g., 0V)	open
	write inhibit bit	VW4 (e.g., 17V)	V3 (e.g., 6V)	open
Writing at Level 2	write bit sense latch: "0" data latch: "~~0~~1" in DL-L, "0" in ~~or~~ DL-R	VW4 (e.g., 17V)	V2 (e.g., 2V)	open
	write inhibit bit	VW4 (e.g., 17V)	V3 (e.g., 6V)	open